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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,935	01/10/2004	Romney R. Katti	H0004883-1600	9236

128 7590 01/12/2006

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EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,935	KATTI, ROMNEY R.	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-23* is/are allowed.

6)☒ Claim(s) *1,3-9,12-17,24 and 25* is/are rejected.

7)☒ Claim(s) *2,10,11,18,19 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 1-8, 24-26 is withdrawn in view of the newly discovered reference(s) to Kouhei et al. (5,515,314). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-6, 8-9, 12, 14, 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Kouhei et al. (5,515,314).

Regarding to claims 1, 3-6, 8, Kouhei et al. disclose a magnetoresistive memory device for applying a bias current to a word line (2, 18) of the memory device to impose a bias field on a magnetoresistive element (6) for centering a hysteresis loop (Fig. 5) of the magnetoresistive element; applying a bias current occurs during a read sequence of the memory device, and wherein the hysteresis loop is a read hysteresis loop (Col. 2, lines 4-20); holding a binary state of the memory device while applying the bias current (Cols. 6, 7, lines 24-58, 6-11, respectively); applying a bias current occurs during a write sequence of the memory device , and wherein the hysteresis loop is a write hysteresis loop (Col. 2, lines 4-20); wherein the memory device is a

giant magnetoresistive memory device (Col. 8, lines 49-65); the bias current is within the approximate range of 5 mA to 40 mA (Col. 8, line 31-41. Also see (Figs. 1-15; Cols. 1-9)

Regarding to claims 9, 12, 14, Kouhei et al. disclose a magnetoresistive memory device comprising: a magnetoresistive element (MR); a word line (2, 18) arranged near the magnetoresistive element for switching a state of the magnetoresistive element and for applying a bias field to the magnetoresistive element (Col. 2, lines 4-20); a bias driver (read/bias means) electrically connected to the word line (2, 18) for applying a bias current to the word line, wherein the bias current being configured to impose a bias field on the magnetoresistive element for centering a hysteresis loop of the magnetoresistive element (Figs. 4-5, 9, lines 11-33); write driver (write means) electrically connected to the word line for applying a switching current to the word line (Cols. 3-4; lines 54-67, 1-11); wherein the magnetoresistive element is a giant magnetoresistive element, anisotropic magnetoresistive element (Col. 8, lines 49-65). Also see (Figs. 1-15; Cols. 1-9)

With regard to claims 24-25, Kouhei et al. disclose a magnetoresistive memory device comprising: a magnetoresistive memory array comprising: a plurality of magnetoresistive memory cells arranged in rows and columns; a plurality of bit lines (16), wherein each bit line aligned in one row and coupled to each memory cell (6) in the row; a plurality of word lines (18), wherein each word line is arranged near a column of memory cells, wherein a current (2) passing through a word line creates a magnetic field acting along an easy axis of each of the memory cells in the column of memory cells; a write driver (write means/circuit) for generating

a write current, wherein the output of the write driver is electrically connected to one or more of the plurality of word lines; and a bias driver (read/bias means), wherein the output of the bias driver is electrically connected to one or more of the plurality of word lines, the bias driver being configured generate a bias current that substantially centers a biased hysteresis loop of a selected magnetoresistive memory cell. (Figs. 4-5, 9, lines 11-33); wherein the write driver is configured to deliver a first current with a first magnitude and a first direction, and the write driver is configured to deliver a second current with a second magnitude and a second direction, wherein the first magnitude is equal to the second magnitude and the first direction is opposite to the second direction. *See Cols. 2-4, lines 4-29, 54-67, 1-11, respectively.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouhei et al. (5,515,314) in view of Ikeda (6,215,695).

With respect to claims 15-16, Kouhei et al. disclose all the elements of the magnetoresistive device applied in claim 9 above.

Kouhei et al. lack an inclusion of wherein the magnetoresistive element comprises a nonmagnetic nonconducting barrier layer sandwiched between two ferromagnetic conducting layers, wherein the coercivety of the first layer is greater than the coercivety of the second layer.

Ikeda discloses a magnetoresistive element comprises a nonmagnetic nonconducting barrier layer (24) sandwiched between first and second ferromagnetic conducting layers (23, 25), wherein the coercivety of the first layer is greater than the coercivety of the second layer. *See Figs. 7, 29-30; Cols. 2, 15, x, lines 32-48, 40-64.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide the magnetoresistive element of Kouhei et al. comprises a nonmagnetic nonconducting barrier layer sandwiched between two ferromagnetic conducting layers, wherein the coercivety of the first layer is greater than the coercivety of the second layer as taught by Ikeda to provide a low cost, reliable, high-speed magnetic memory device.

4. Claims 7, 13, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouhei et al. (5,515,314) in view of Nguyen et al. (6,888,742).

With respect to claim 17, Kouhei et al. disclose all the elements of the magnetoresistive device applied in claim 9 above.

Kouhei et al. Lack an inclusion of wherein the magnetoresistive element comprising a magnetic tunneling junction; an antiferromagnetic layer; a ferromagnetic pinned layer coupled to the antiferromagnetic layer; a nonmagnetic conducting layer coupled to the pinned layer, and a ferromagnetic free layer coupled to the nonmagnetic conducting layer.

Nguyen et al. disclose a magnetoresistive element comprising a magnetic tunneling junction; an antiferromagnetic layer (102); a ferromagnetic pinned layer (104) coupled to the antiferromagnetic layer; a nonmagnetic conducting layer (106) coupled to the pinned layer, and a ferromagnetic free layer (108) coupled to the nonmagnetic conducting layer. *See Fig. 3; Col. 8, lines 4-42.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide magnetoresistive element of Kouhei et al. comprising a magnetic tunneling junction; an antiferromagnetic layer; a ferromagnetic pinned layer coupled to the antiferromagnetic layer; a nonmagnetic conducting layer coupled to the pinned layer, and a ferromagnetic free layer coupled to the nonmagnetic conducting layer as taught by Nguyen et al. in order to provide a low-power consumption and high-speed magnetic memory device.

Allowable Subject Matter

5. Claims 2, 10-11, 18-19, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the method steps of claim 1 and further comprising step of in response to a determination, triggering a rewrite to restore the memory device to the first state, and among others claimed in claim 2; the magnetoresistive memory of claim 9, and wherein the bias driver, among other as claimed in claims 10, 11, configured to apply the bias current during write/read cycle of the magnetoresistive device; the magnetoresistive memory of claim 24, and further comprises means for returning the magnetoresistive element to the first state in response to a determination, and among others as claimed in claim 18, 19; the magnetoresistive memory of claim 24 and the interconnection between write driver, bias driver, write line, switch and word line as claimed in claim 26.

6. The following is an examiner's statement of reasons for allowance: Claims 20-23 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: a magnetoresistive memory device comprising: a word line electrically isolated from a primary and complementary magnetoresistive elements, a current, among others as claimed in independent claim 20, in the word line cause a magnetic field to be applied to the primary and complementary magnetoresistive elements; wherein the magnetic field of the primary element is same magnitude and opposite direction of the complementary magnetoresistive element.

Response to Arguments

Applicant's arguments, file on 11/1/05 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kouhei et al. (5,515,314).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID LAM
PRIMARY EXAMINER

D. Lam

January 2, 2006